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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/812,282	03/30/2004	Yasutaka Nakashiba	8008-1052	2273

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EXAMINER	
JACKSON JR, JEROME	

ART UNIT	PAPER NUMBER
2815	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/812,282	NAKASHIBA, YASUTAKA	
	Examiner	Art Unit	
	Jerome Jackson Jr.	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 June 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-22 are rejected under 35 U.S.C. 102(e) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Kudo 6,853,037.

Kudo shows multiple transistors with different gate oxide thicknesses in wells of opposite conductivity to the substrate. The advantage is low power consumption combined with high speed circuitry. The claims are broadly written with functional language and statements of intended use and do not structurally distinguish over Kudo regardless of the intended use of the transistors as "varactors" or MOS transistors. See

the previously recited caselaw on functional language. The limitations "about" and connections to "ground" do not structurally distinguish over Kudo where voltages connected to the same regions in Kudo may likewise be labeled "ground" and the dimensions of Kudo's device is similarly "about" the same. Furthermore, in the event the claims are amended to positively recite exact voltages and connections for all the regions of the "varactors" disclosed in the specification, connecting MOS transistors to form varactor devices was well known in the art as evidenced by applicant's prior art admissions. It cannot be considered a patentable step in the art to practice either MOSFET transistor device of Kudo as a "varactor" because one of ordinary skill would be led to practice a FET as a varactor and choose either transistor according to the varactor voltage required to form a VCO oscillator circuit from applicant's admitted prior art. The advantages of having MOS transistors of different thresholds is disclosed by Kudo. The advantage of practicing a varactor from the same transistors used as other CMOS circuitry already on the chip and used for other purposes such as memory cells, input/output devices, etc. is also established. A mere combination of all the expected results of using the existing CMOS transistors on the chip for several purposes to increase integration, complexity, and likewise improve reliability, size, etc. is substantial motivation to use the existing chip CMOS for as many circuits as possible. Accordingly, applicant's invention cannot be considered patentable absent unexpected results of which there are none now evident.

Claims 1-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kudo in view of O 7,088,964.

O teaches integrating an entire system on a single chip. The backround and specification also teach CMOS for varactors or VCO's in the system. Kudo suggests multiple transistor gate oxide transistors to enable transistors of different threshold voltage and different functions for the various circuitry of the O system circuitry while improving power consumption and device speed. The increased process complexity is balanced against the improved reliability and smaller size, etc. of integrated circuitry. Integrating CMOS as Kudo to make a system on a chip as O with VCO's incorporating CMOS transistors is considered obvious to one of ordinary skill for the advantages inherent in maximum "integration" on a single chip. Applicant's claim structure is obvious in view of the teachings and suggestions of Kudo and O.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jerome Jackson Jr. whose telephone number is 571-272-1730. The examiner can normally be reached on M-Th.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

jj

JEROME JACKSON
PRIMARY EXAMINER